IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application : **10/581,117**

Applicant(s) : **van GASSEL et al.**

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Examiner : **SNYDER, Steven G.**

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Title: **POWER SAVING METHOD AND SYSTEM**

Mail Stop: **APPEAL BRIEF - PATENTS**
Commissioner for Patents
Alexandria, VA 22313-1450

APPEAL UNDER 37 CFR 41.37

Sir:

This is an appeal from the decision of the Examiner dated 22 July 2008, finally rejecting claims 1-20 of the subject application.

This paper includes (each beginning on a separate sheet):

1. **Appeal Brief;**
2. **Claims Appendix;**
3. **Evidence Appendix; and**
4. **Related Proceedings Appendix.**

APPEAL BRIEF

I. REAL PARTY IN INTEREST

The above-identified application is assigned, in its entirety, to **Koninklijke Philips Electronics N. V.**

II. RELATED APPEALS AND INTERFERENCES

Appellant is not aware of any co-pending appeal or interference that will directly affect, or be directly affected by, or have any bearing on, the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-20 are pending in the application.

Claims 1-20 stand rejected by the Examiner under 35 U.S.C. 103(a).

These rejected claims are the subject of this appeal.

IV. STATUS OF AMENDMENTS

No amendments were filed subsequent to the final rejection in the Office Action dated 22 July 2008. A reply to the final rejection was filed on 17 September 2008.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention addresses a method and system for conserving power in a device that includes buffer memory that is coupled to a mass storage device (Applicants' page 1, lines 2-5). The applicants have recognized that conventional power saving schemes that minimize the power consumed by memory elements may be sub-optimal, particularly when these memory elements are used as a buffer for a mass storage device (page 5, lines 1-9). As illustrated in the applicants' FIG. 1, the power consumed by a memory element (SDRAM) increases with the size of the memory, whereas if the memory is used as a buffer for a mass storage device

(HDD), the power consumed by the mass storage device decreases with the size of the buffer memory; accordingly, there is an optimal size of memory for reducing the total power consumed by the combination of the memory element and the mass storage device (page 4, lines 14-29). Further, the mass storage device's power consumption, and the savings achievable by increasing the size of the buffer memory, is also dependent upon other factors, primarily the rate at which data is transferred between the mass storage device and the buffer memory (page 4, lines 9-14), which is often dependent upon the particular application being executed on the host device (page 5, lines 1-4).

As claimed in independent claim 1, the invention comprises a method for adaptively minimizing the total power consumption of an apparatus comprising a subsystem (FIG. 2; page 4, lines 1-2) comprising a mass storage device (21) and a buffer memory (22), said method comprising the steps of (FIG. 3):

determining (33) an optimum buffer size for which the power consumption of said subsystem is a minimum for a given streaming bit-rate to/from said buffer memory (page 5, lines 10-16), and

adjusting (34) the buffer size of said buffer memory to said optimum buffer size, such that the power consumption of said subsystem is minimal (page 5, lines 18-19).

As claimed in dependent claim 3 and 14, the invention comprises the method according to claims 1 and 2, respectively, wherein the storage device is a hard disk drive and the step of determining an optimum buffer size comprises:

determining (31) a hard disk drive data rate (page 5, lines 11-12),

determining (32) the stream bit-rate to/from the buffer memory (page 5, lines 12-14), and

determining (33) the optimum buffer size having the lowest power consumption at the determined stream bit-rate (page 5, lines 14-18).

As claimed in dependent claims 5, 15, 16, 17, and 18 the invention comprises the method according to claims 1, 14, 2, 3, and 4, respectively, wherein the optimum buffer size is determined by the ratio of the stream bit rate and the disk bit rate giving the duty cycle of the hard disk drive for calculating/estimating the hard disk drive power consumption, which subsequently is used to determine the optimal buffer size (page 4, lines 14-17).

As claimed in dependent claims 7 and 19, the invention comprises the method according to claims 1 and 2, respectively, wherein a powering down of a memory bank or IC is either delayed or the buffered data of that memory bank or IC is moved to another memory bank that will remain powered on after which the first bank is shut down immediately, when a stream is stopped and removed (page 6, lines 30-34).

As claimed in independent claim 9, the invention comprises (FIG. 4) a circuit (42) for retrieving data from a mass storage device (48) via a memory buffer (43, 44) comprising a processing unit conceived to:

- adaptively (46) activate or deactivate areas of said buffer memory in such a manner that total power consumption of a subsystem comprising said storage device and said buffer memory is minimized for a given streaming rate to/from said buffer memory (page 6, lines 17-20); and
- retrieve the data from the mass storage device (page 6, lines 4-6).

As claimed in independent claim 13, the invention comprises (FIG. 5) a computer-readable medium (5) having embodied thereon a computer program for processing by a computer (55), the computer program comprising code segments for adaptively minimizing the total power consumption of a subsystem comprising a mass storage device and a buffer memory, wherein

a first code segment (58) determines an optimum buffer size for which the power consumption of said subsystem is a minimum for a given streaming bit-rate from said buffer memory (page 7, lines 23-24), and

a second code segment (59) adjusts the buffer size of said buffer memory to said optimum buffer size, such that the power consumption of said subsystem is minimal (page 7, lines 24-26).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-4, 6, 9-14, and 20 stand rejected under 35 U.S.C. 103(a) over Kever et al. (USPA 2003/0145239, hereinafter Kever) and Korst et al. (USP 6,016,732, hereinafter Korst).

Claims 5 and 15-18 stand rejected under 35 U.S.C. 103(a) over 103(a) over Kever, Korst, and Kling et al. (USPA 2001/0003207, hereinafter Kling).

Claims 7 and 19 stand rejected under 35 U.S.C. 103(a) over Kever, Korst, and Yoshida (USP 5,928,365).

VII. ARGUMENT

Claims 1-4, 6, 9-14, and 20 stand rejected under 35 U.S.C. 103(a) over Kever and Korst

Claims 1-4, 6, 13-14, and 20

The combination of Kever and Korst fails to disclose determining an optimum buffer size for which the power consumption of a subsystem comprising a mass storage device and a buffer memory is a minimum for a given streaming bit-rate to/from said buffer memory, as claimed in claim 1, upon which claims 2-8 and 14-20 depend. Independent claim 13 includes similar features.

The Examiner asserts that Kever teaches determining an optimum buffer size for which the power consumption of a subsystem comprising a mass storage device and a buffer memory is a minimum at paragraphs [0009]-[0010] (Office action, page 5, last 5 lines). The applicants respectfully disagree with this assertion. At the cited text, Kever teaches:

> "When a software application is compiled, a signal may be sent from the software application to the PMU to indicate how much L3 cache memory the application may need. The PMU then turns on the appropriate amount of cache memory needed for that application.

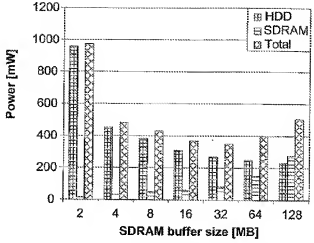
> While a software application is running, the application may also send a signal to the PMU to indicate how much L3 cache memory the application needs at that time." (Kever, [0009]-[0010].)

As is readily apparent, the above cited text does not address the power consumed by a mass storage device and a buffer memory, and specifically does not teach determining an optimum buffer size for which the power consumption of a subsystem comprising a mass storage device and a buffer memory is a minimum, as asserted by the Examiner.

Kever teaches turning off as much memory as possible to reduce power consumption. This reduction is controlled in two ways: memory that is not accessed for a defined time is turned off, and, only memory that an application requires is turned on (Kever's Abstract, last 7 lines). Kever does not address the power consumed by a mass storage device, and the Examiner fails to identify where Kever teaches minimimizing the power consumed by the combination of a mass storage device and a buffer memory, as specifically claimed by the applicants.

In the Advisory Action of 29 September 2008, the Examiner acknowledges that Kever teaches minimizing the power consumption of a buffer memory, and asserts that "any further system that includes this buffer memory would inherently benefit from the minimizing of the power consumption" (Advisory action, page 2, lines 4-5). This assertion is incorrect.

As illustrated in the applicants' FIG. 1, below, the power consumed by a buffer memory is minimized by minimizing the size of the buffer. However, minimizing the size of the buffer does not minimize the power consumed by the combination of a mass storage device and the memory buffer, as specifically claimed by the applicants. The optimum buffer size for minimizing the power consumed by the combination of the mass storage device and the buffer memory is not the buffer size that minimizes the power consumption of the buffer memory.



As illustrated in the example above, the power consumed by an 8MB memory buffer (SDRAM) is less than the power consumed by a 16MB or 32MB memory buffer; however, the total power consumed in this example is less if a 16MB or 32MB memory buffer is used instead of an 8MB buffer. In this example, the optimum buffer size is 32MB. At a slower data transfer rate, the power consumed by the mass storage device will decrease, eventually to a point where the optimal size of the buffer becomes 16MB, and with a further decrease in data transfer rate, a buffer size of 8MB may be optimal.

Kever does not address the power consumed by a mass storage device, and cannot be said to select an optimal buffer size based on this power consumption, as taught and claimed by the applicants. Korst also does not address the power consumed by a mass storage device, and does not cure this deficiency in Kever.

Because Kever fails to disclose determining an optimum buffer size for which the power consumption of a subsystem comprising a mass storage device and a buffer memory is a minimum, and because the Examiner fails to identify where either Kever of Korst teaches controlling a buffer size based on the power consumed by a combination of mass storage device and buffer memory, the applicants respectfully maintain that the rejection of claims 1-4, 6, 13-14, and 20 under 35 U.S.C. 103(a) over Kever and Korst is unfounded, and should be reversed by the Board.

Claims 9-12

The combination of Kever and Korst fails to disclose adaptively activating or deactivating areas of a buffer memory in such a manner that total power consumption of a subsystem comprising a storage device and a buffer memory is minimized for a given streaming rate to/from the buffer memory, as claimed in claim 9, upon which claims 10-12 depend.

In this rejection, the Examiner relies on the basis of the rejection of claim 1 for rejecting claim 9 (Office action, page 10, lines 1-3). As noted above, the combination of Kever and Korst fails to teach the elements of claim 1; accordingly, the applicants respectfully maintain that the rejection of claims 9-12 under 35 U.S.C. 103(a) over Kever and Korst is unfounded, and should be reversed by the Board.

Claims 3-4 and 14

The combination of Kever and Korst fails to disclose determining a hard disk drive data rate, determining the stream bit-rate to/from the buffer memory, and determining the optimum buffer size having the lowest power consumption at the determined stream bit-rate, as claimed in claim 3, upon which claim 4 depends, and claim 14.

The Examiner acknowledges that Kever does not teach determining a hard disk drive data rate, determining the stream bit-rate to/from the buffer memory, and determining the optimum buffer size having the lowest power consumption at the determined stream bit-rate, and asserts that Korst provides this teaching at column 2, lines 21-45 and column 5, line 66 - column 6, line 7. The applicants respectfully disagree with this assertion.

At column 2, lines 21-45, Korst teaches techniques for assuring that there is always a sufficient amount of data in a set of buffers to avoid underflow, or stalling. At column 5, line 66 - column 6, line 7, Korst teaches a scheduling scheme for fetching data blocks to provide to the buffers. At neither cite does Korst address power consumption, and specifically does not teach determining an optimum buffer size having a lowest power consumption, as claimed by the applicants.

Because the combination of Kever and Korst fails to disclose determining an optimum buffer size having the lowest power consumption at a determined stream bit-rate, the applicants respectfully maintain that the rejection of claims 3-4 and 14 under 35 U.S.C. 103(a) over Kever and Korst is unfounded, and should be reversed by the Board.

Claims 5 and 15-18 stand rejected under 35 U.S.C. 103(a) over Kever, Korst, and Kling

Claims 5 and 15-18

Each of claims 5 and 15-18 is dependent upon claim 1, and in this rejection, the Examiner relies on the combination of Kever and Korst for teaching the elements of claim 1. As detailed above, the combination of Kever and Korst fails to teach the elements of claim 1; accordingly, the applicants respectfully maintain that the rejection of claims 5 and 15-18 under 35 U.S.C. 103(a) that relies on the combination of Kever and Korst for teaching the elements of claim 1 is unfounded, and should be reversed by the Board.

Further, the combination of Kever, Korst, and Kling fails to disclose determining an optimum buffer size based on a ratio of the stream bit rate and the disk bit rate of the hard disk drive as specifically claimed in each of claims 5 and 15-18.

The Examiner acknowledges that Kever does not provide this teaching, and asserts that Kling provides this teaching at paragraph [0018]. The applicants respectfully disagree with this assertion. At the cited text, Kling teaches:

> "In accordance with an embodiment of the present invention, the power consumed by at least a portion of a computer system is monitored by measuring a parameter that is approximately proportional to the consumed power, such as voltage, current, or the duty cycle of a switching signal in a power supply. These measurements are provided to a power controller. The portion of the computer system that is monitored may include one or more processors of the computer system in addition to other integrated circuits (ICs) that consume a significant amount of power such as, for example, the bridge (or "chipset") or the video terminal." (Kling [0018].)

As is clearly evident, at the cited text, Kling fails to address determining a ratio of a stream bit rate and a disk bit rate, and specifically fails to disclose determining an optimum buffer size based on this ratio.

Because the combination of Kever, Korst, and Kling fails to disclose determining an optimum buffer size based on a ratio of the stream bit rate and the disk bit rate of the hard disk drive, the applicants respectfully maintain that the rejection of claims 5 and 15-18 under 35 U.S.C. 103(a) over Kever, Korst, and Kling is unfounded, and should be reversed by the Board.

Claims 15 and 17-18

Claim 15 is dependent upon claim 14, and claims 17-18 are dependent upon claim 3. The Examiner fails to address this dependency, and presumably relies upon the combination of Kever and Korst for teaching the elements of claims 3 and 14.

As noted above, the combination of Kever and Korst fails to disclose the elements of claims 3 and 14. The applicants also maintain that Kling does not address the elements of claims 3 and 14, and the Examiner does not identify where Kling teaches the elements of claims 3 and 14. Accordingly, the applicants respectfully maintain that the rejection of claims 15 and 17-18 under 35 U.S.C. 103(a) over Kever, Korst, and Kling is unfounded, and should be reversed by the Board.

Claims 7 and 19 stand rejected under 35 U.S.C. 103(a) over Kever, Korst, and Yoshida

Claims 7, 19

Each of claims 7 and 19 is dependent upon claim 1, and in this rejection, the Examiner relies on the combination of Kever and Korst for teaching the elements of claim 1. As detailed above, the combination of Kever and Korst fails to teach the elements of claim 1; accordingly, the applicants respectfully maintain that the rejection of claims 7 and 19 under 35 U.S.C. 103(a) that relies on the combination of Kever and Korst for teaching the elements of claim 1 is unfounded, and should be reversed by the Board.

CONCLUSIONS

Because neither Kever, Korst, Kling, or Yoshida addresses determining an optimal buffer size based on the power consumed by a subsystem comprising a mass storage device and a buffer memory, the applicants respectfully request that the Examiner's rejection of claims 1-20 under 35 U.S.C. 103(a) be reversed by the Board, and the claims be allowed to pass to issue.

Because the Examiner fails to identify where the prior art teaches the elements of dependent claims 3-5 and 14-18, as detailed above, the applicants respectfully request that the Examiner's rejection of each of claims 3-5 and 14-18 under 35 U.S.C. 103(a) be reversed by the Board, and the claims be allowed to pass to issue.

Respectfully submitted

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CLAIMS APPENDIX

1. A method for adaptively minimising the total power consumption of an apparatus comprising a subsystem comprising a mass storage device and a buffer memory, said method comprising the steps of

determining an optimum buffer size for which the power consumption of said subsystem is a minimum for a given streaming bit-rate to/from said buffer memory, and

adjusting the buffer size of said buffer memory to said optimum buffer size, such that the power consumption of said subsystem is minimal.

2. The method according to claim 1, wherein said step of adjusting the buffer size comprises switching on memory banks and/or memory ICs of said buffer memory for increasing the size of said buffer memory, and switching off memory banks and/or memory ICs for decreasing said buffer memory.

3. The method according to claim 1, wherein the storage device is a harddisk drive and the step of determining an optimum buffer size comprises

determining a harddisk drive data rate,

determining the stream bit-rate to/from the buffer memory, and

determining the optimum buffer size having the lowest power consumption at the determined stream bit-rate.

4. The method according to claim 3, wherein said optimum buffer size determination step comprises calculating optimum buffer size from a formula, looking up optimum buffer size in a look-up table, or measuring the minimum power consumption of the subsystem in a feedback loop controlling buffer size.

5. The method according to claim 1, wherein the optimum buffer size is determined by the ratio of the stream bit rate and the disk bit rate giving the duty cycle of the harddisk drive for calculating/estimating the harddisk drive power consumption, which subsequently is used to determine the optimal buffer size.

6. The method according to claim 1 comprising powering up extra memory banks and/or memory ICs when a new stream is admitted.

7. The method according to claim 1, wherein a powering down of a memory bank or IC is either delayed or the buffered data of that memory bank or IC is moved to another memory bank that will remain powered on after which the first bank is shut down immediately, when a stream is stopped and removed.

8. The method according to claim 1, wherein in case of multiple simultaneous streams, the sum of the bit-rates of all streams is determined.

9. A circuit for retrieving data from a mass storage device via a memory buffer comprising a processing unit conceived to:

- adaptively activate or deactivate areas of said buffer memory in such a manner that total power consumption of a subsystem comprising said storage device and said buffer memory is minimised for a given streaming rate to/from said buffer memory; and
- retrieve the data from the mass storage device.

10. An apparatus comprising a subsystem comprising mass storage device, a buffer memory and the circuit according to claim 9.

11. The apparatus according to claim 10, wherein said buffer memory comprises SDRAM circuits having banks of memory adapted to be independently switched on/off.

12. The apparatus according to claim 10, wherein a scheduler function executable by the processing unit controls accessing the storage device and the buffer memory.

13. A computer-readable medium having embodied thereon a computer program for processing by a computer, the computer program comprising code segments for adaptively minimising the total power consumption of a subsystem comprising a mass storage device and a buffer memory, wherein

a first code segment determines an optimum buffer size for which the power consumption of said subsystem is a minimum for a given streaming bit-rate from said buffer memory, and

a second code segment adjusts the buffer size of said buffer memory to said optimum buffer size, such that the power consumption of said subsystem is minimal.

14. The method according to claim 2, wherein the storage device is a harddisk drive and the step of determining an optimum buffer size comprises

determining a harddisk drive data rate,

determining the stream bit-rate to/from the buffer memory, and

determining the optimum buffer size having the lowest power consumption at the determined stream bit-rate.

15. The method according to claim 14, wherein the optimum buffer size is determined by the ratio of the stream bit rate and the disk bit rate giving the duty cycle of the harddisk drive for calculating/estimating the harddisk drive power consumption, which subsequently is used to determine the optimal buffer size.

16. The method according to claim 2, wherein the optimum buffer size is determined by the ratio of the stream bit rate and the disk bit rate giving the duty cycle of the harddisk drive for calculating/estimating the harddisk drive power consumption, which subsequently is used to determine the optimal buffer size.

17. The method according to claim 3, wherein the optimum buffer size is determined by the ratio of the stream bit rate and the disk bit rate giving the duty cycle of the harddisk drive for calculating/estimating the harddisk drive power consumption, which subsequently is used to determine the optimal buffer size.

18. The method according to claim 4, wherein the optimum buffer size is determined by the ratio of the stream bit rate and the disk bit rate giving the duty cycle of the harddisk drive for calculating/estimating the harddisk drive power consumption, which subsequently is used to determine the optimal buffer size.

19. The method according to claim 2, wherein a powering down of a memory bank or IC is either delayed or the buffered data of that memory bank or IC is moved to another memory bank that will remain powered on, after which the first bank is shut down immediately when a stream is stopped and removed.

20. The apparatus according to claim 11, wherein a scheduler function executable by the processing unit controls accessing the storage device and the buffer memory.

EVIDENCE APPENDIX

No evidence has been submitted that is relied upon by the appellant in this appeal.

RELATED PROCEEDINGS APPENDIX

Appellant is not aware of any co-pending appeal or interference which will directly affect or be directly affected by or have any bearing on the Board's decision in the pending appeal.